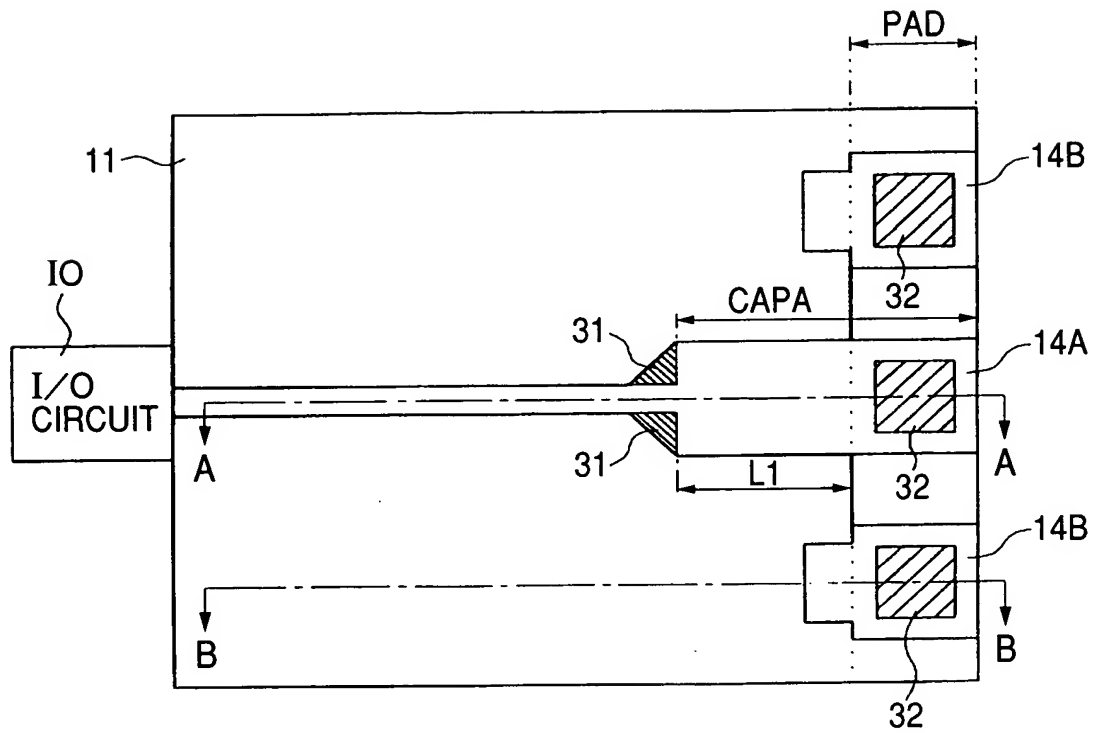


FIG. 1

11 : FIRST-LAYER WIRING (FIRST WIRING)
 14A : FOURTH-LAYER WIRING (FOURTH WIRING)

FIG. 2

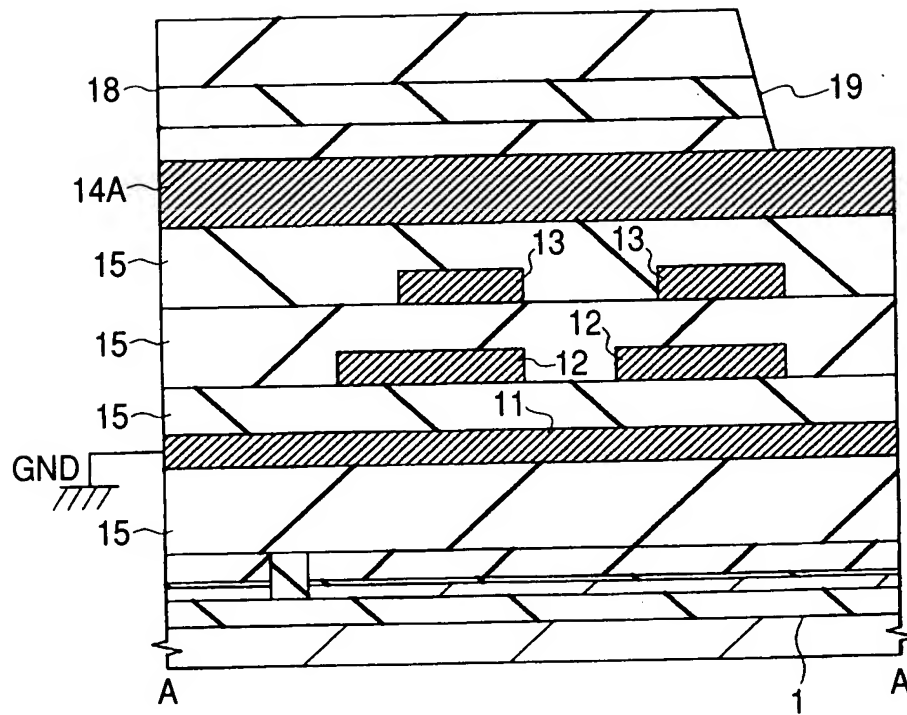


FIG. 3

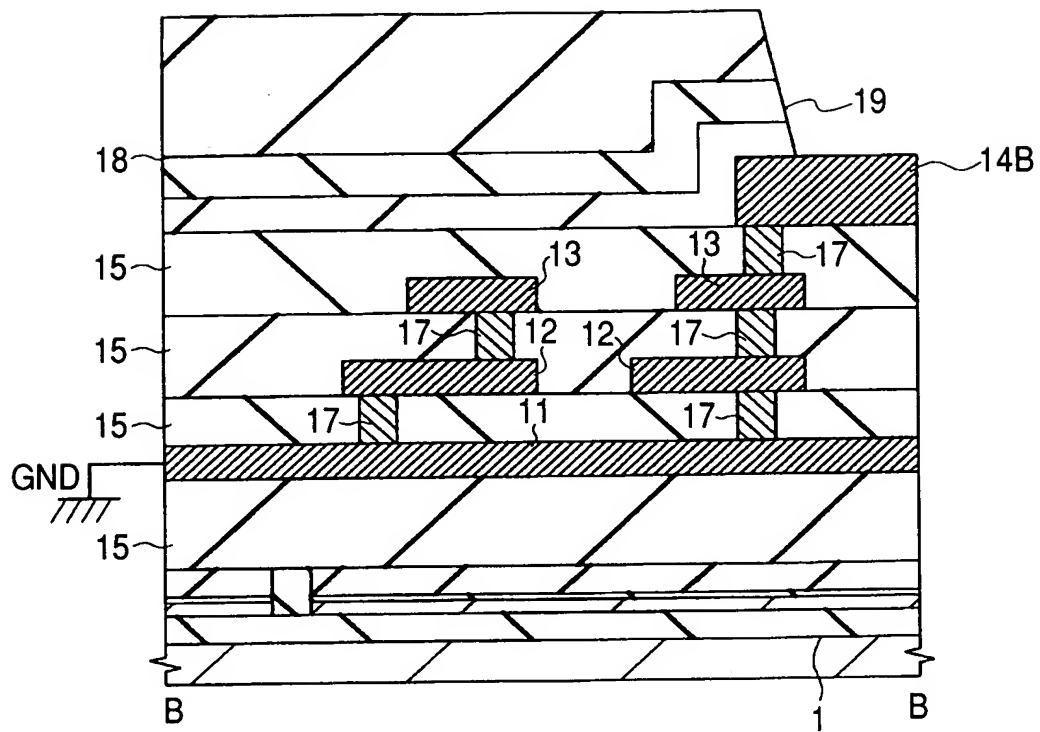


FIG. 4

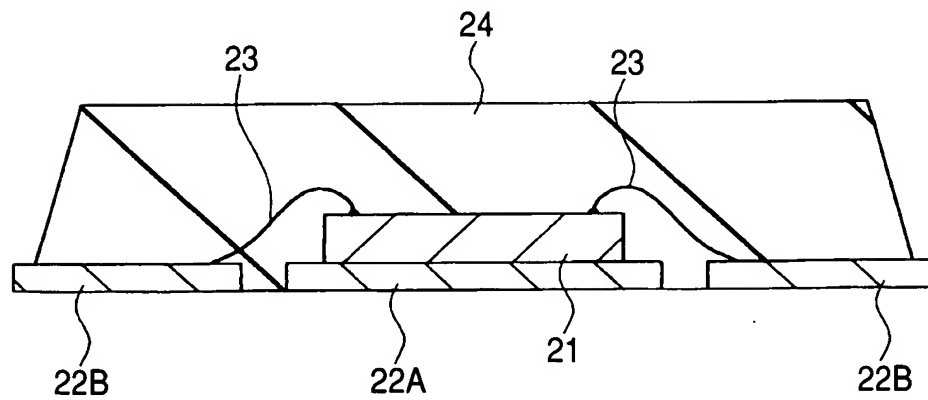
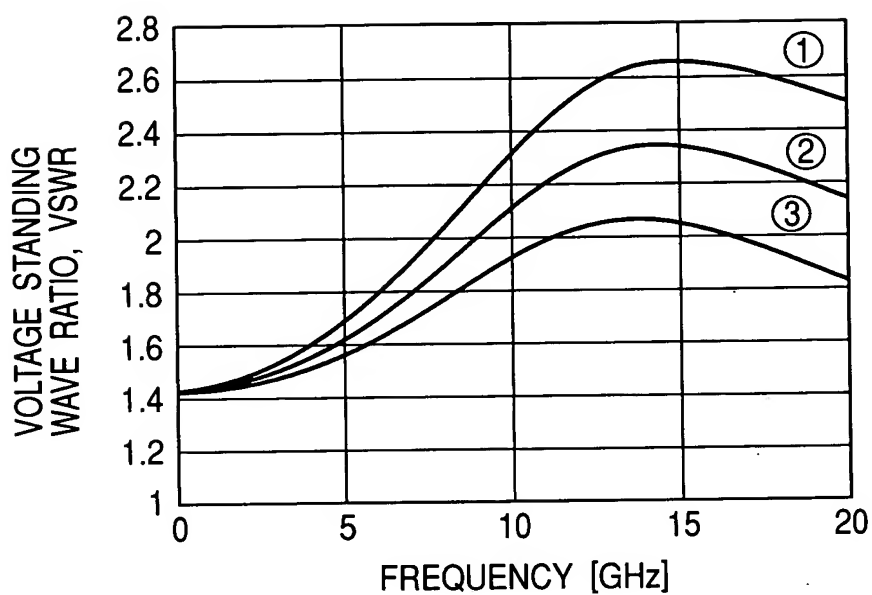


FIG. 5

WIRE INDUCTANCE : 1nH

No.	L	VSWR ($\leq 12\text{GHz}$)	TRANSMISSION LOSS ($\leq 12\text{GHz}$)	DECISION	REASON
①	$0\ \mu\text{m}$	2.7	-0.1dB	×	LARGE VSWR
②	$50\ \mu\text{m}$	2.4	-0.3dB	○	MOST SUITABLE
③	$100\ \mu\text{m}$	2.1	-0.5dB	×	LARGE LOSS

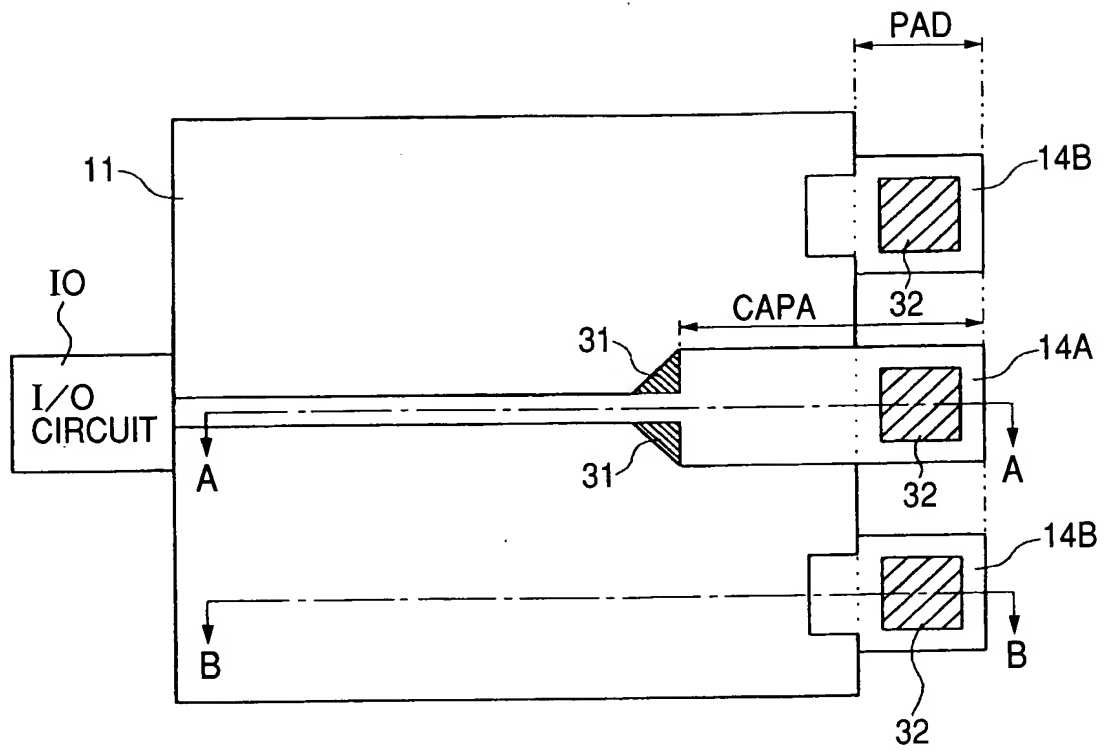
FIG. 6

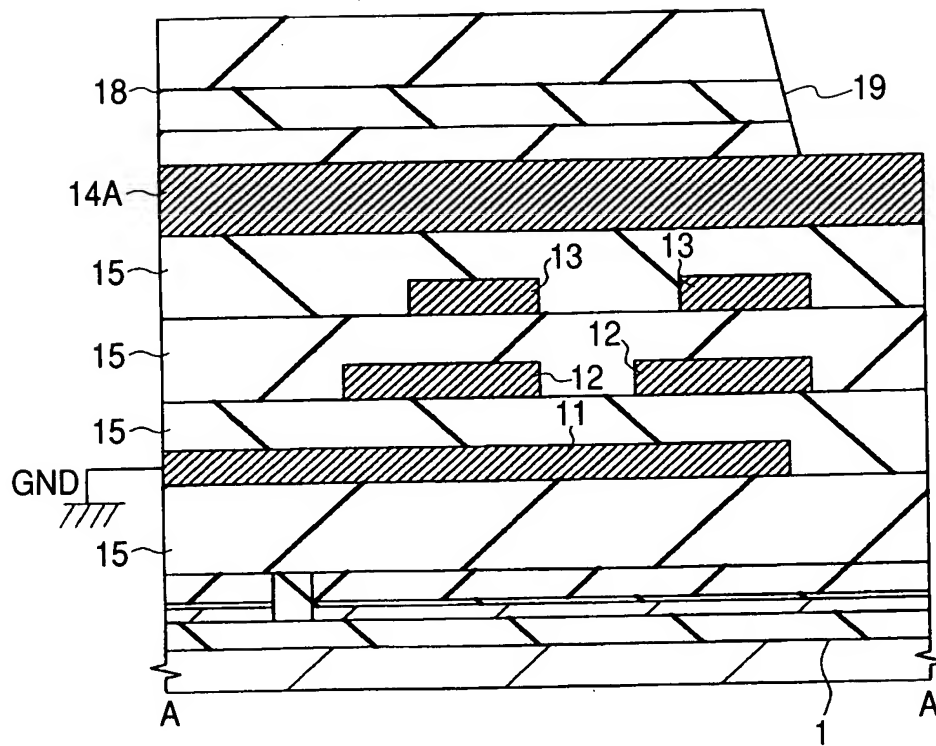
FIG. 7

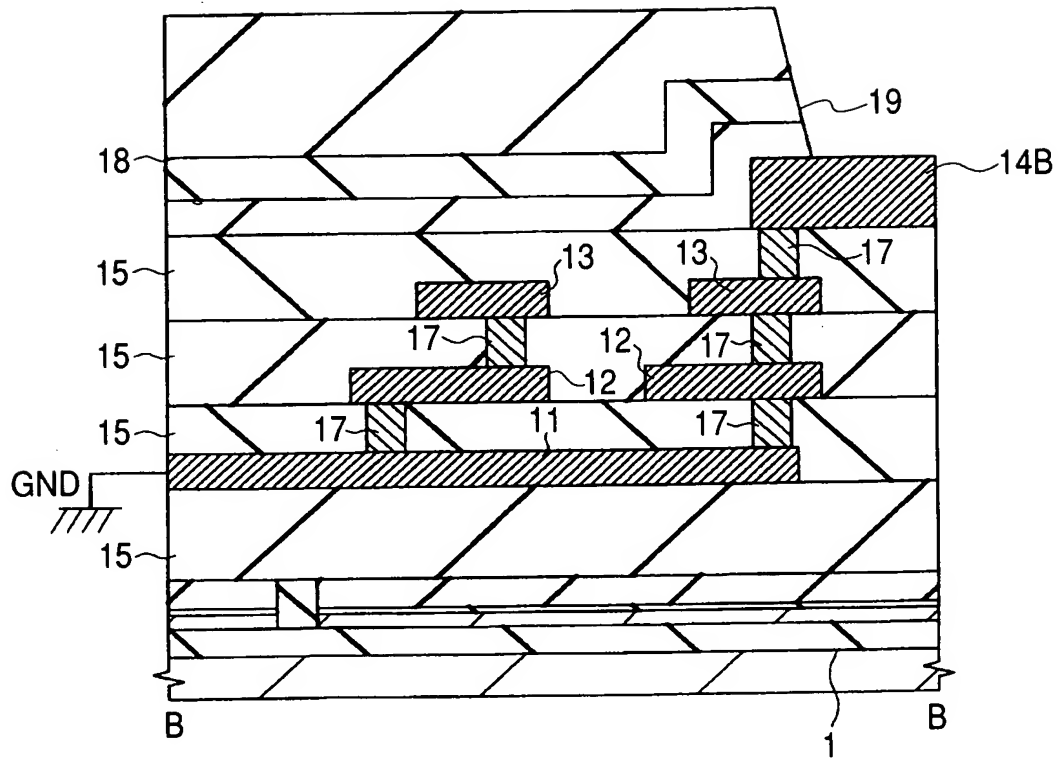
FIG. 8

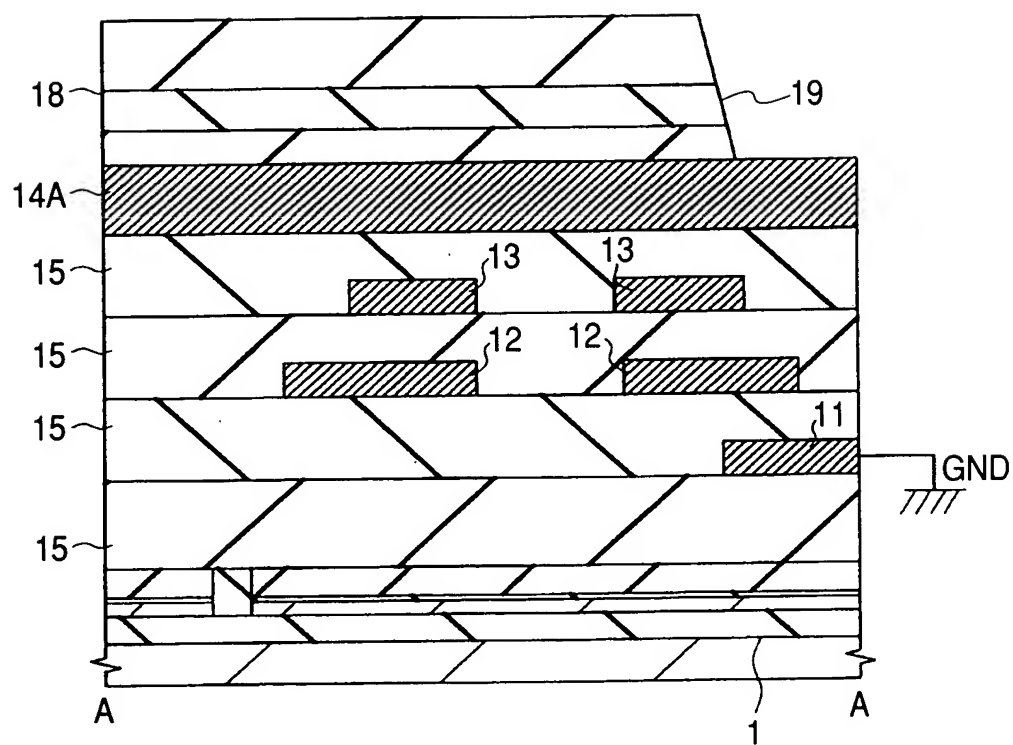
FIG. 10

FIG. 12

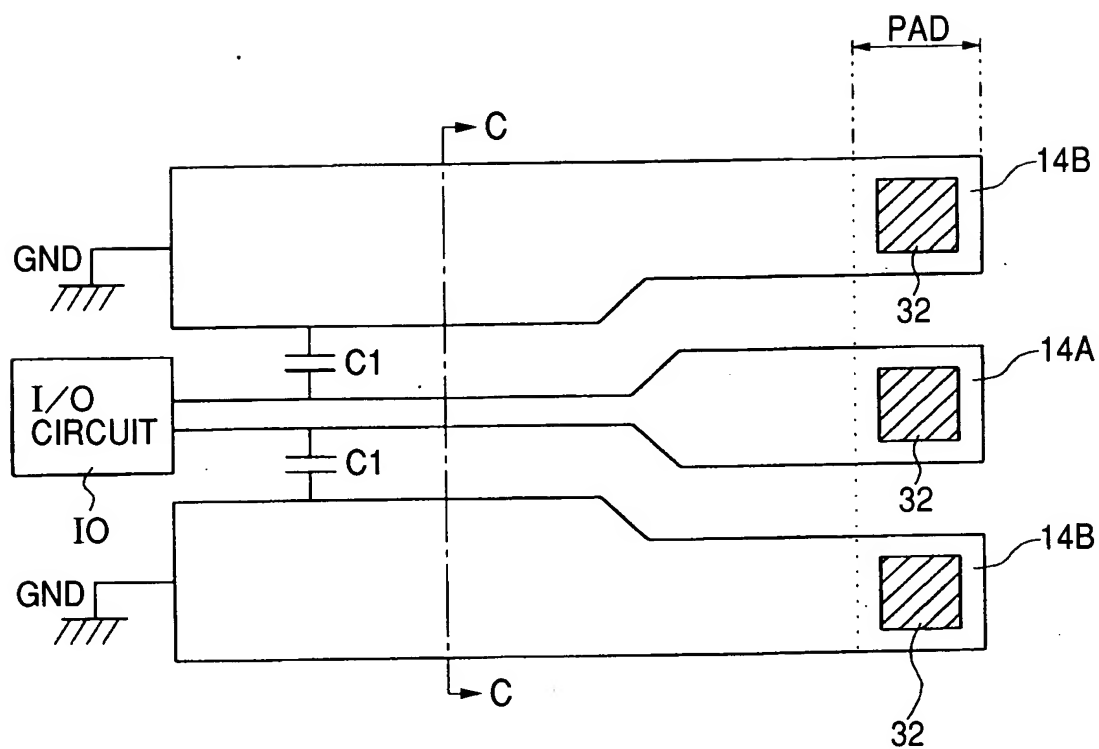


FIG. 13

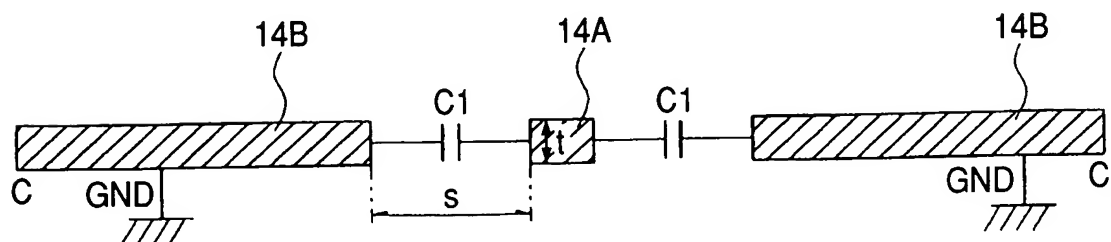


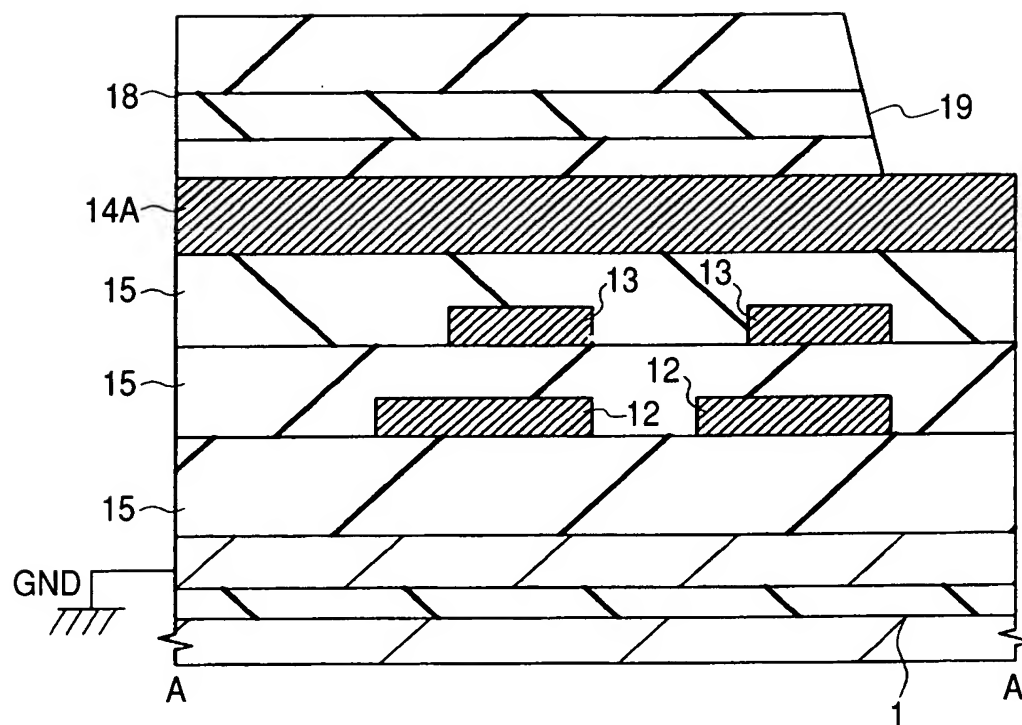
FIG. 14

FIG. 15

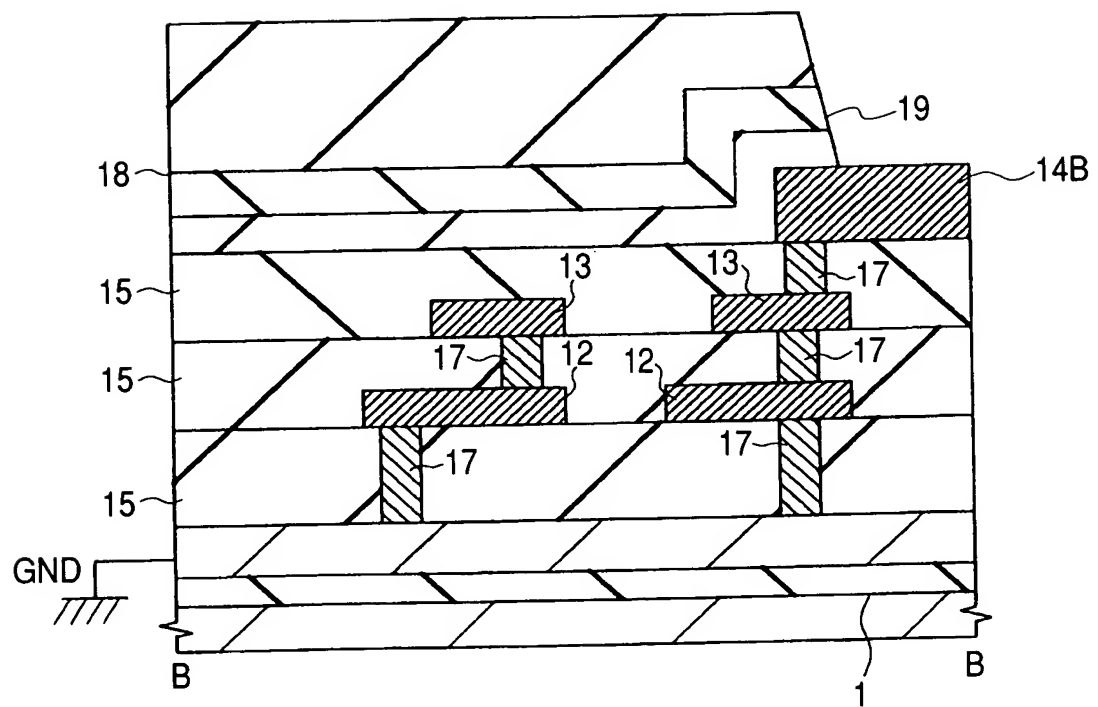


FIG. 16

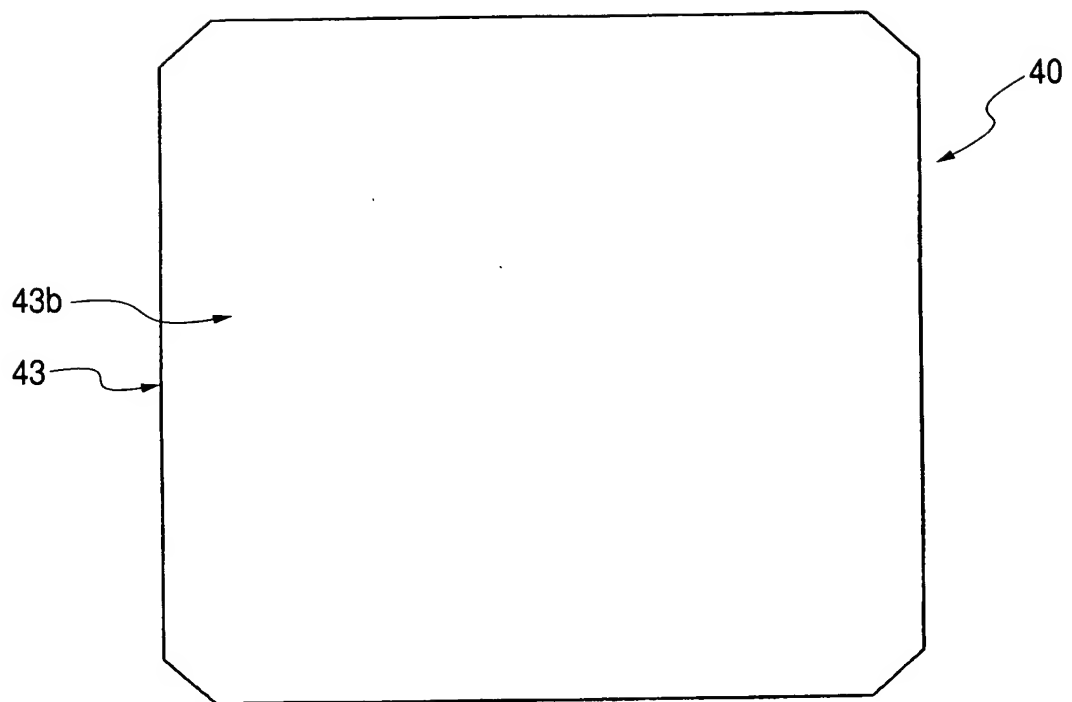


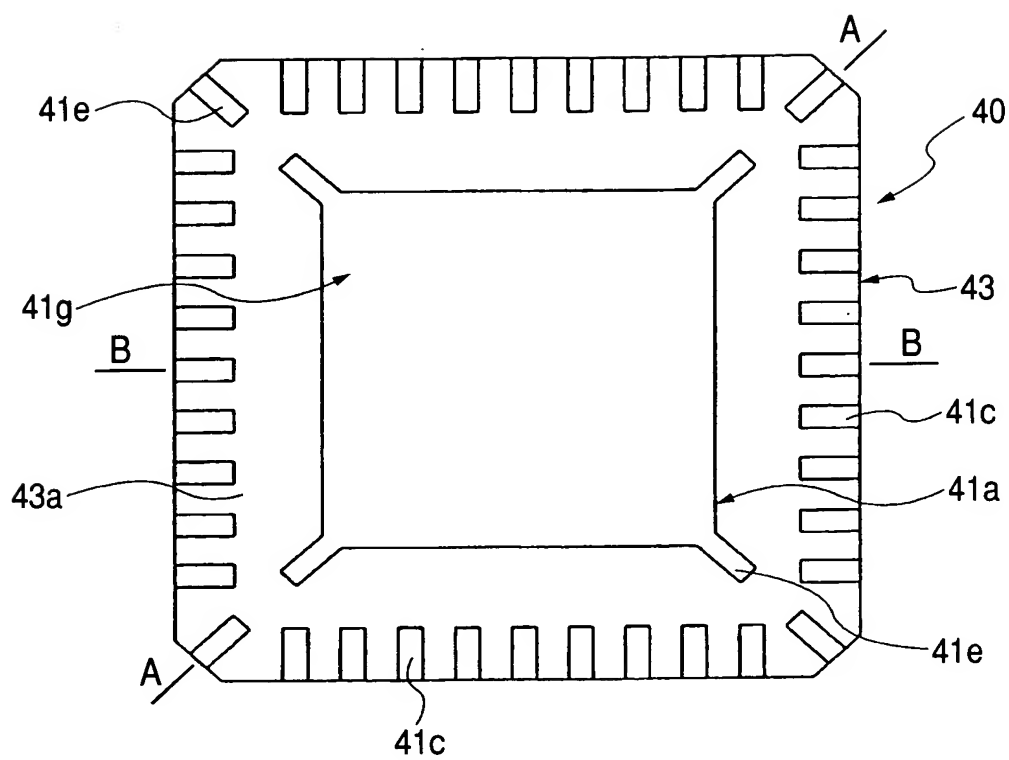
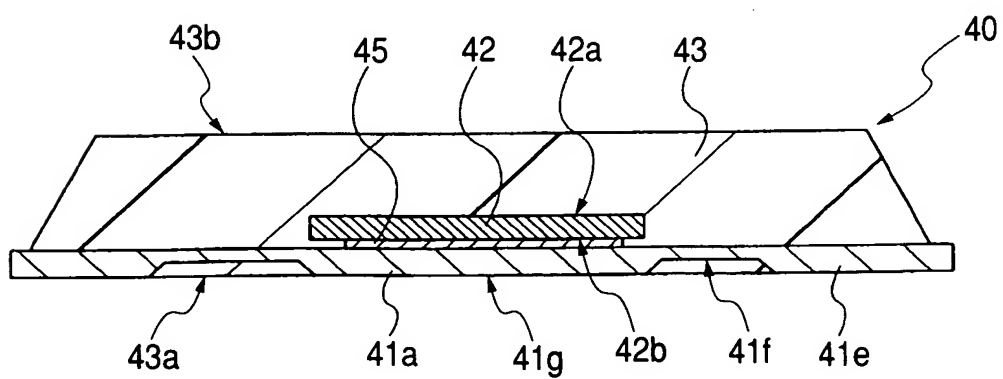
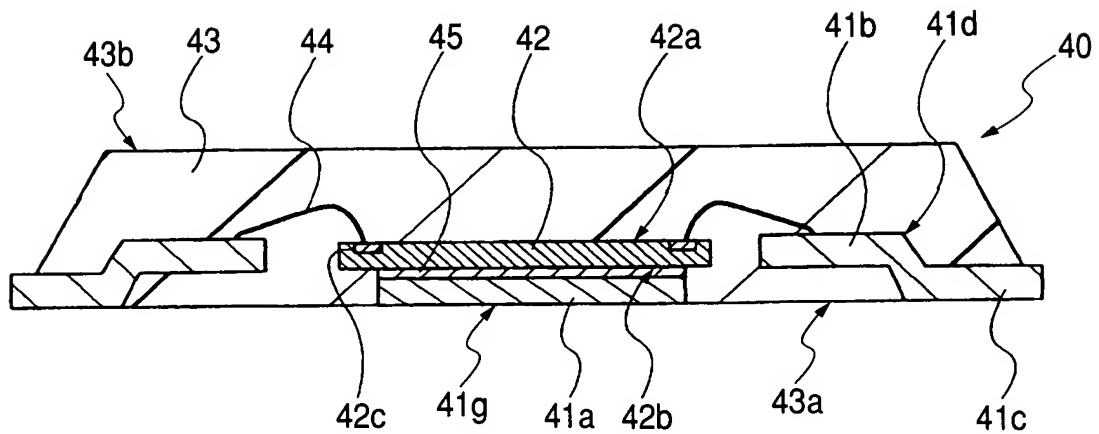
FIG. 17**FIG. 18**

FIG. 19



- 40 : QFN (SEMICONDUCTOR DEVICE)
- 41a : DIE PAD
- 41b : INNER LEAD PORTION
- 41c : OUTER TERMINAL PORTION
- 41d : LEAD
- 42 : SEMICONDUCTOR CHIP
- 42a : MAIN SURFACE
- 42b : BACK SURFACE
- 42c : BONDING PAD (ELECTRODE)
- 43 : SEALING MEMBER
- 43a : MOUNTING SURFACE
- 43b : SURFACE (OPPOSITE SIDE)
- 44 : BONDING WIRE

FIG. 21

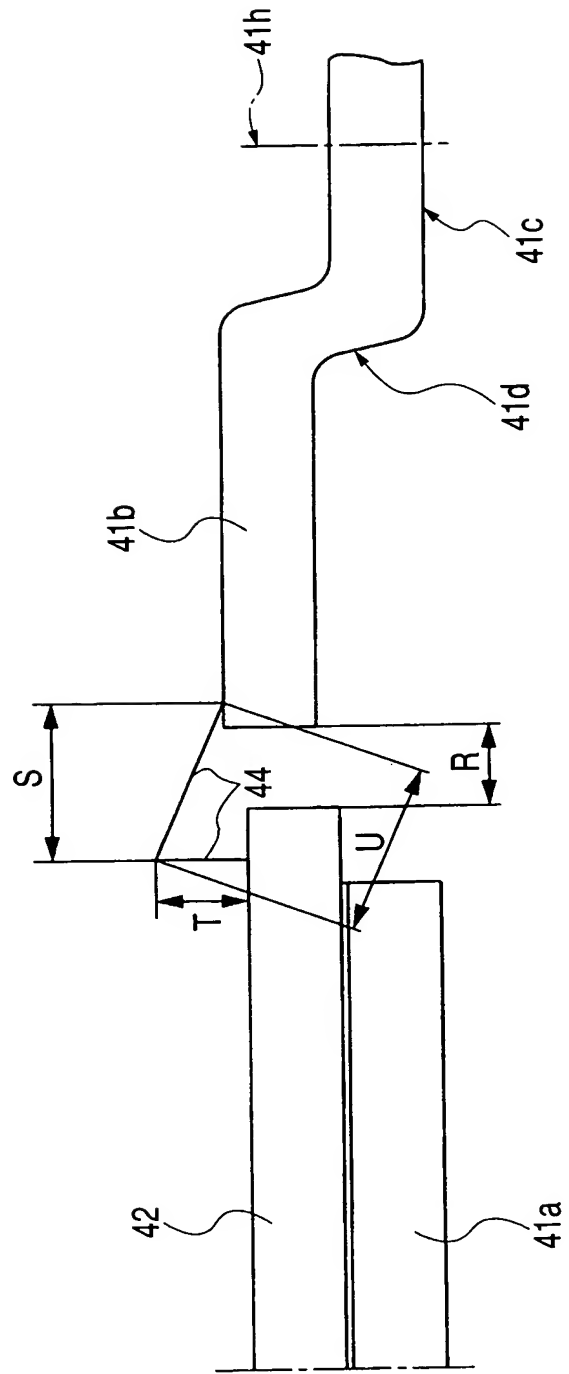


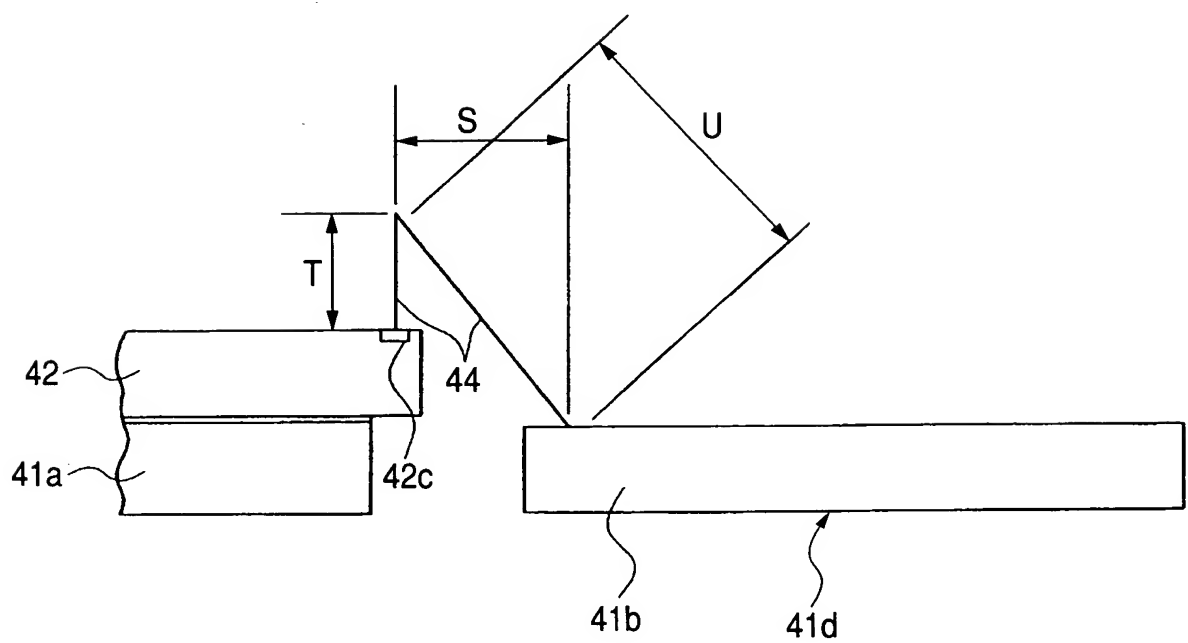
FIG. 22

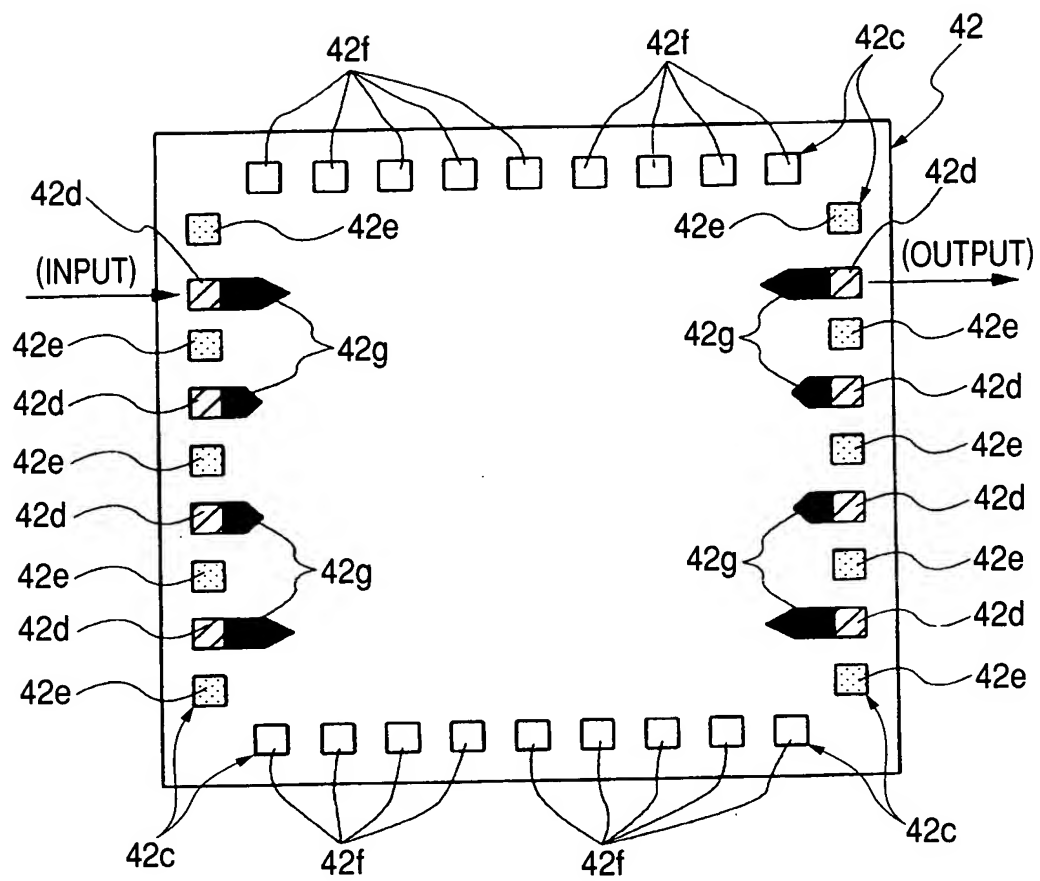
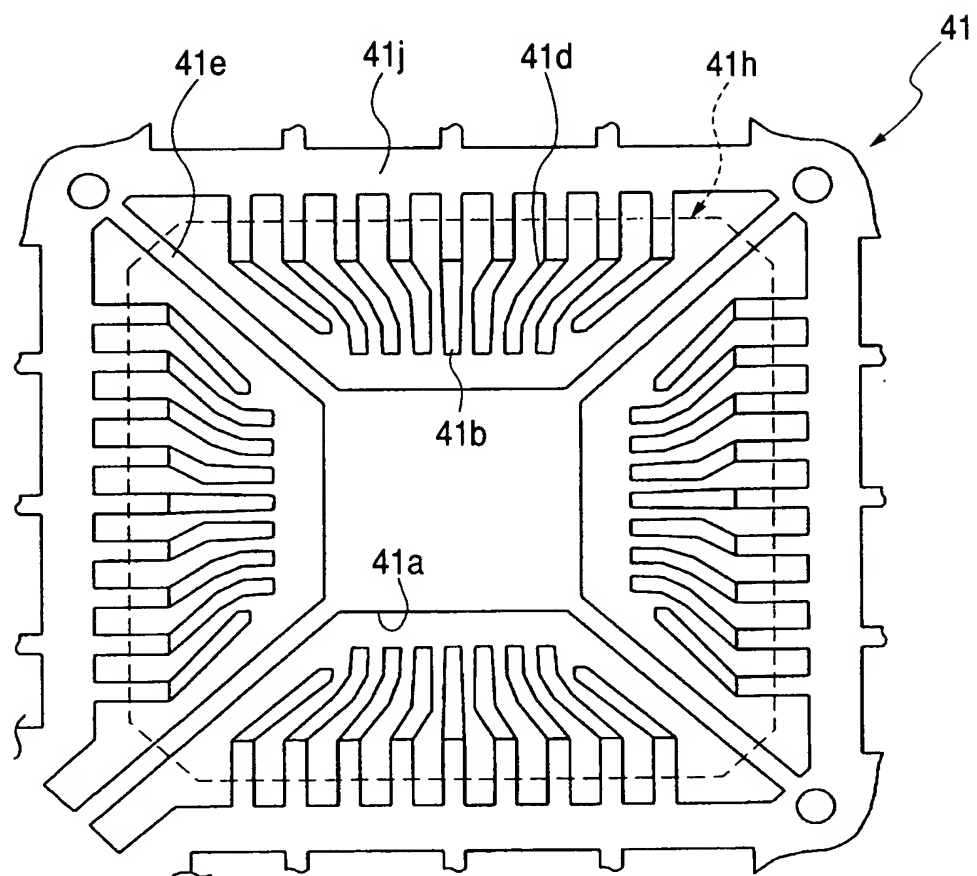
FIG. 23

FIG. 24



41 : LEAD FRAME

FIG. 25

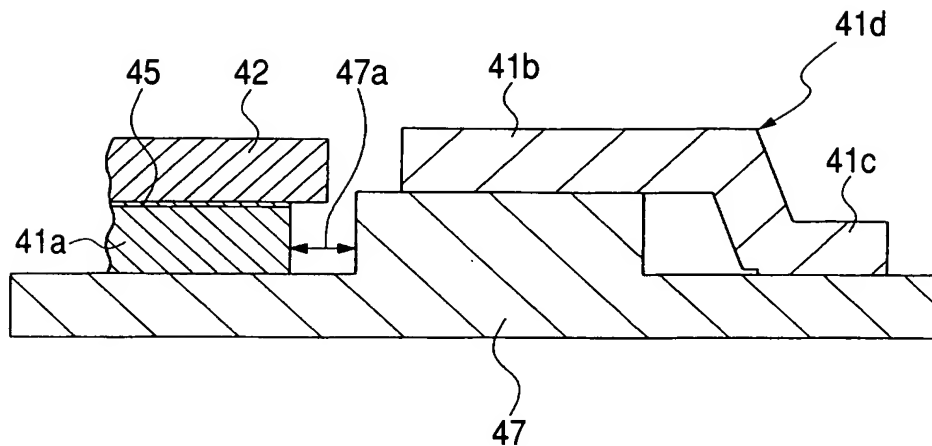


FIG. 26

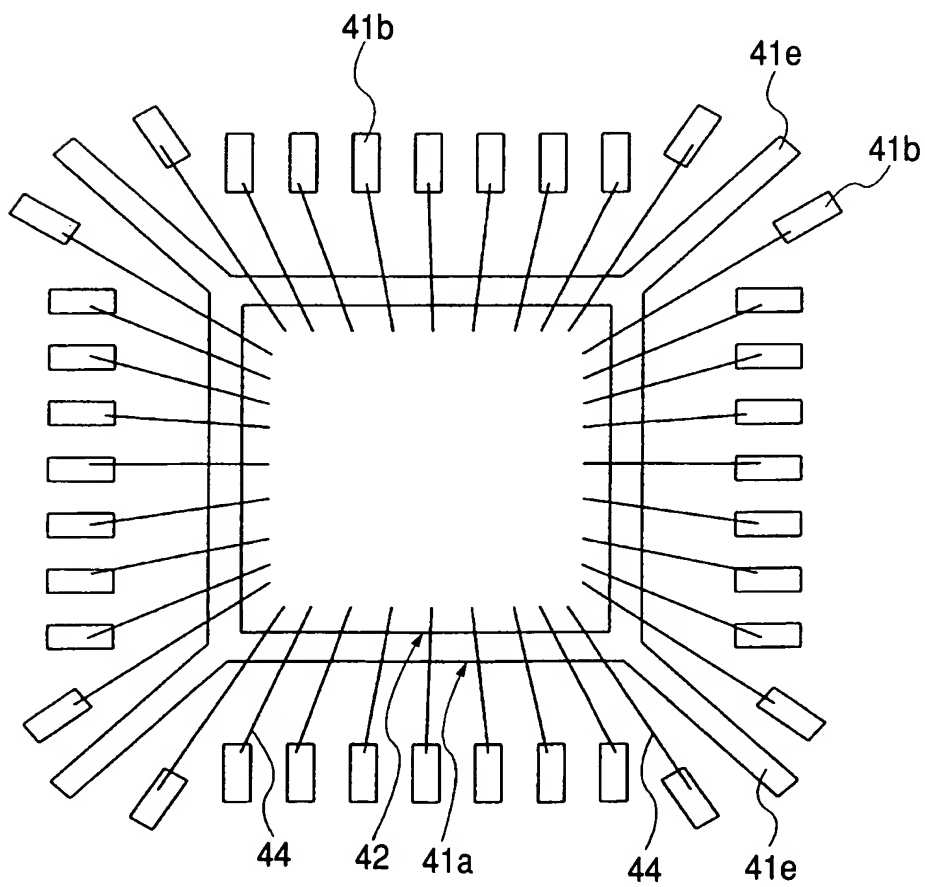


FIG. 27

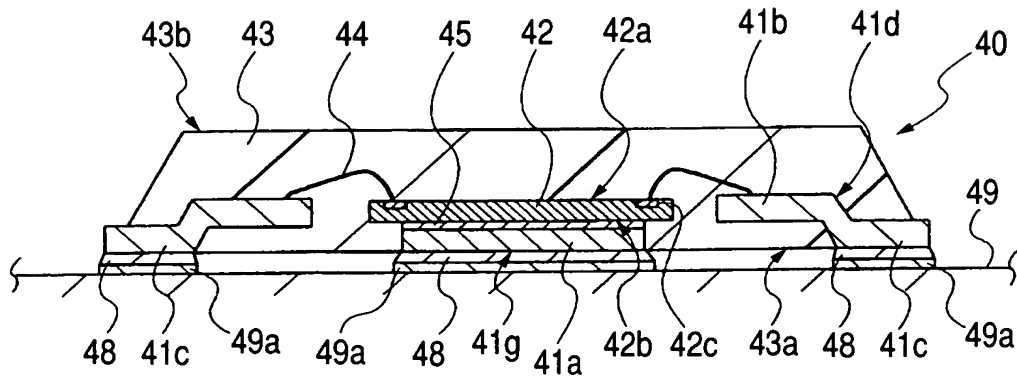
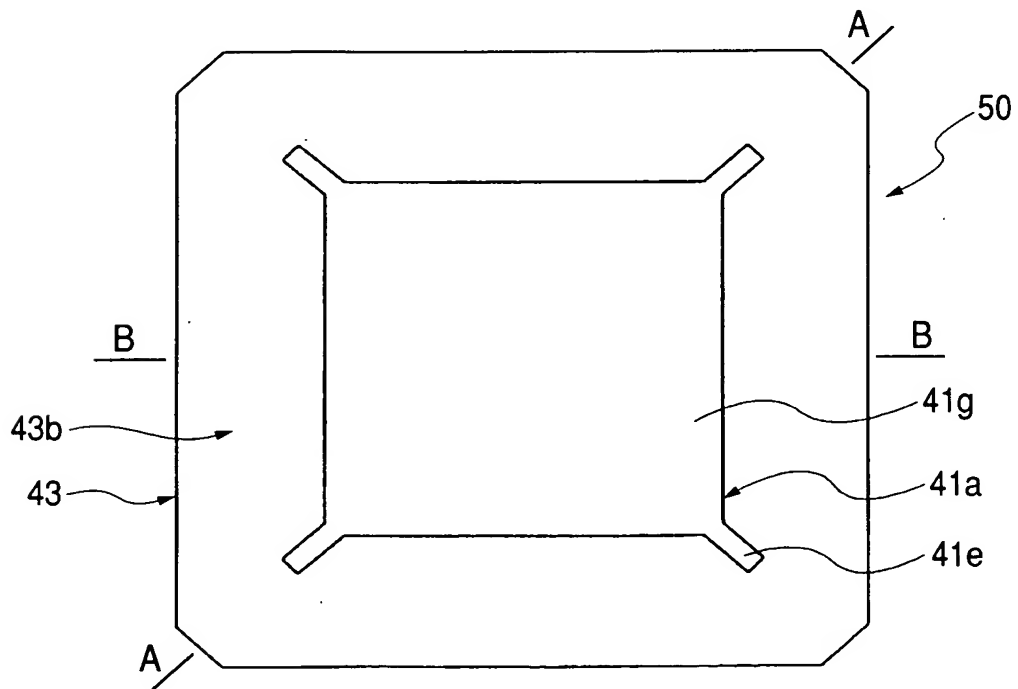


FIG. 28



50 : QFN (SEMICONDUCTOR DEVICE)

FIG. 29

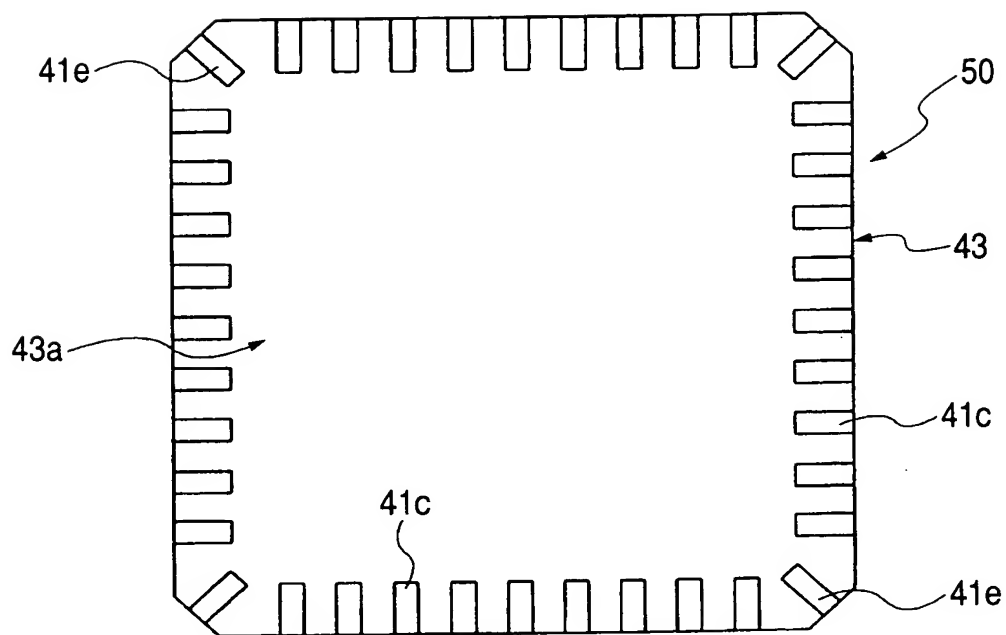
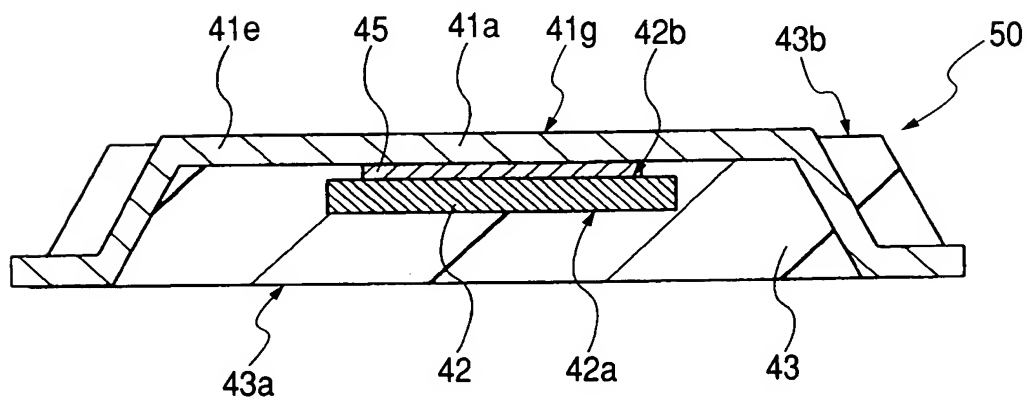
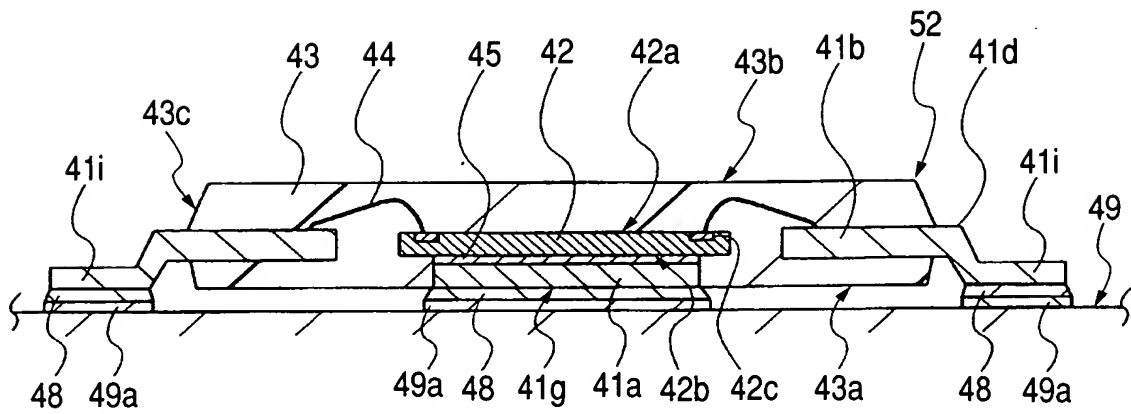


FIG. 30



This cross-sectional view shows a semiconductor device 50. A central layer 41a is positioned on a base 42. A gate 42b is formed on top of layer 41a. The device is surrounded by various layers: 41b on the top, 41c on the bottom, and 41d on the sides. A layer 43 is located on the left and right sides, with sub-layers 43a and 43b. A layer 44 is on the left, and a layer 45 is on the right. A layer 42a is located between the base 42 and the central layer 41a.

FIG. 33



41i : OUTER LEAD (OUTER TERMINAL PORTTION)

43c : SIDE FACE

52 : QFP (SEMICONDUCTOR DEVICE)